

## Using Mentor Questa® for pre-silicon validation

### of IEEE 1149.1-2013 based Silicon Instruments

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#### Introduction

IEEE 1149.1-2013 is not your father's JTAG. The new release in June of 2013 represents a major leap forward in standardizing how FPGAs, SoCs and 3D-SICs can be debugged and tested. The standard defines register level descriptions of on-chip IP with operational descriptions via the new 1149.1 Procedural Description Language.<sup>1,2,3</sup> IEEE 1149.1-2013 adds support for TAP based access to on-chip IP, configuring I/O parameters such as differential voltage swing, crossing power domains and controlling on-chip power, segmented scan chains and interfacing into IEEE 1500 Wrapper Serial Ports and WIRs. The standard is architected to lower the cost of electronic products by enabling re-use of on-chip instruments through all phases of the IC life-cycle. The standard takes a 'divide and conquer' approach allowing IP (instrument) providers who have the most domain expertise of their IP to communicate the structure and operation of their IP in computer readable formats.

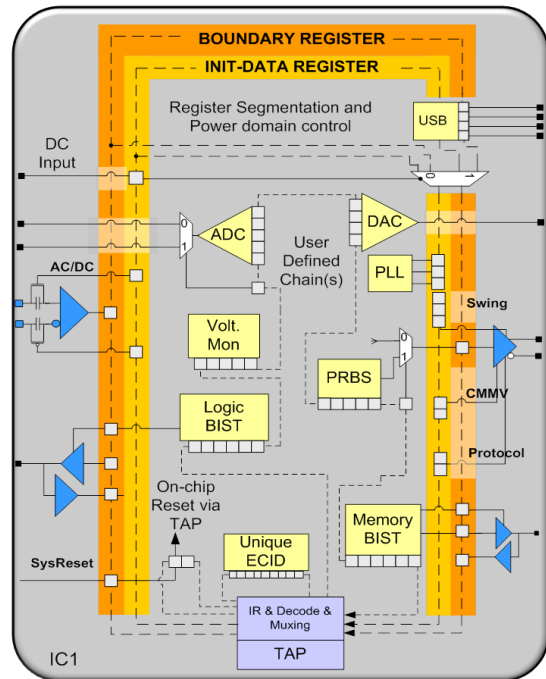


Figure 1. Example IEEE-1149.1-2013 IC

IC integrators can then plug-n-play this IP into a design and leverage pre-written and pre-verified operation with low cost 1149.1 based tools. The end user does not need to read datasheets and develop Verilog or C/C++ code to operate the provided instrument. Figure 1. shows an example IC with a number of TAP accessible instruments such as Logic BIST, PRBS generator, Memory BIST, Voltage and temperature monitors, PLL, Analog-to-Digital converters, Digital to Analog converters. Many other types of TAP (Test Access Port) accessible instrumentation exist, such as bus monitors, droop injectors, external DDR memory, SERDES BER testers and FPGA-based universal instruments.<sup>4</sup> Intellitech refers to the many flavors of on-chip IP for test and debug as "Silicon Instruments™".

<sup>1</sup> [IEEE 1149.1-2013 - IEEE Standard for Test Access Port and Boundary Scan Architecture.](#)

<sup>2</sup> [IEEE 1149.1™-2013 Designed to Slash Electronics Industry Costs by Allowing Test Re-Use Throughout Integrated Circuit Lifecycle](#)

<sup>3</sup> [Tutorial on IEEE 1149.1-2013 Internal JTAG](#)

<sup>4</sup> ["FPGA-based universal embedded digital instrument", Josh Ferry, ITC 2013 Proceedings](#)

## The Problem

Test benches in Verilog have been the de facto approach to validating JTAG architectures since 1990 when some of the first ICs with on-chip instruments were created. This approach works, but in a limited way. The Verilog test bench may operate the JTAG interface in a way which is not the way the interface is used with JTAG based debuggers or PCB testers. The Verilog test benches also perhaps were not delivered to the customer and certainly not supplied to the IC end user who could benefit from TAP based access to the on-chip features. An example is the OEM system designer who wants to characterize his FR4 design early on and needs access to TAP based SERDES BER (Bit Error Rate Test).

The PDL (Procedure Definition Language) introduced in IEEE 1149.1-2013 changes the validation approach. The IP or silicon provider now needs to validate the PDL routines against the product being delivered. Ideally this is done during simulation rather than after tape-out. Pre-silicon validation ensures that the design's instrumentation can be configured via the TAP and that the descriptions in BSDL and PDL will do their job correctly when first silicon is available. During first silicon bring up, linear time is critical, it's not the time to be debugging PDL code or being unsure if the on-chip instrument works as planned.

The major roadblock in developing pre-validated instrument control descriptions in PDL is that commercial simulators don't know how to read IEEE 1149.1-2013 PDL or instrument package descriptions.

## The Approach

Questa® and ModelSim® customers can use a freely available software front-end from Intellitech called NEBULA to process the IEEE 1149.1-2013 file formats and drive the simulators.<sup>5</sup> Figure 2 shows the integration which allows pre-silicon validation and post silicon use.

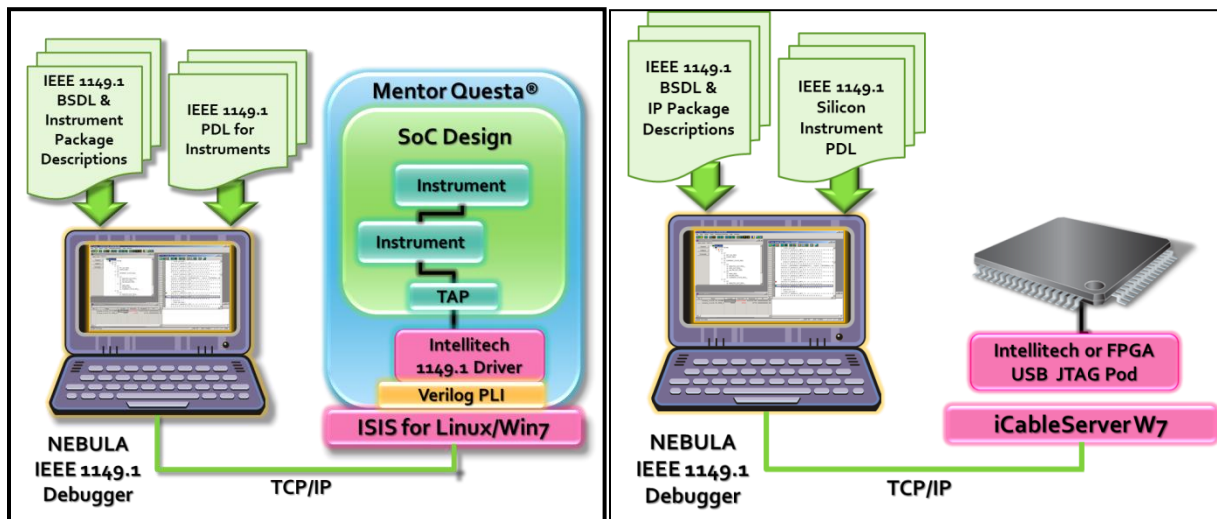


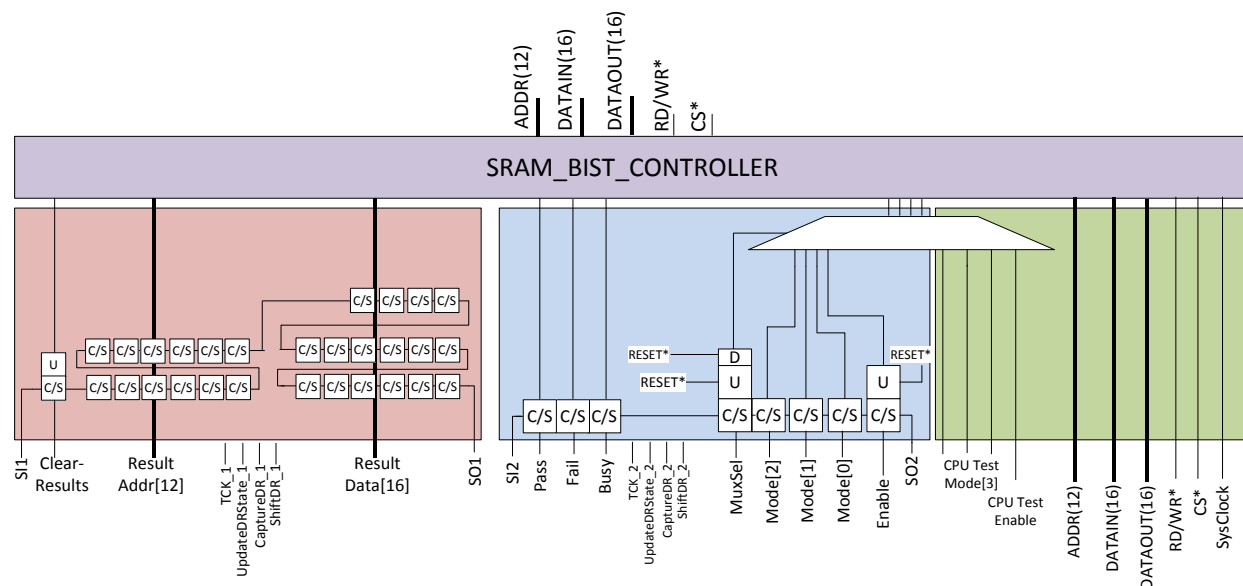
Figure 2: NEBULA to Questa® Interface and NEBULA to 1149.1 Pod Interface

<sup>5</sup> [Intellitech NEBULA software](#)

To validate any Silicon Instrument™, the engineer uses Questa® to compile the Verilog of the instrument and links in the Intellitech supplied ISIS (Intellitech Simulation Interface Server) DLL (Dynamic Link Library) or Linux SO (Shared Object) File. ISIS allows the Intellitech NEBULA client software to send and receive data to and from the design following the IEEE 1149.1 protocol. It performs a similar function as Intellitech's iCableServer software does when a user has a USB based JTAG cable connected to an actual IC.

This validation process of the instrument and any data/control paths from the IEEE 1149.1 I/O pins saves valuable time during the testing of initial silicon. The validation identifies all peripheral signals, such as system clocks and resets, which are required for TAP-based control and proper operation of the instrument.

While there are many useful instruments with various level of complexity, this article uses a simple SRAM Built-In Self-Test (BIST) as a test instrument to demonstrate the value of using Questa® to validate the IP description and PDL. Figure 3 shows a block diagram of the instrument that includes an IEEE 1149.1-2013 compliant wrapper. The 1149.1-2013 approach is designed to allow instruments to plug-and-play by connecting compatible TDRs together; it also reduces the support burden for the IP provider as the complete instrument with mission mode control paths can be delivered to the instrument customer.



**Figure 3. SRAM Test Instrument with 1149.1-2013 interface**

The mission mode interface is shown in the shaded green. Access to the SRAM is performed through the SRAM\_BIST\_Controller block through an internal mux. A CPU interface is provided which enables the on-chip CPU to access the instrument in exactly the same way as the 1149.1-2013 interface enables the interface. The blue shaded section provides the control and status of the SRAM\_BIST capabilities via an 1149.1-2013 TDR (Test Data Register) segment. IEEE 1149.1-2013 has standardized on using TDRs compatible with IEEE 1500, that is, using the capture, shift and update states with free running TCK rather than the original specification which used gated clock. For FPGA compatibility, we also developed the SRAM instrument interface to support gated TCK operation. While IEEE 1500 style is preferred, the TAP controller in some FPGAs uses a gated clock interface. If you are developing

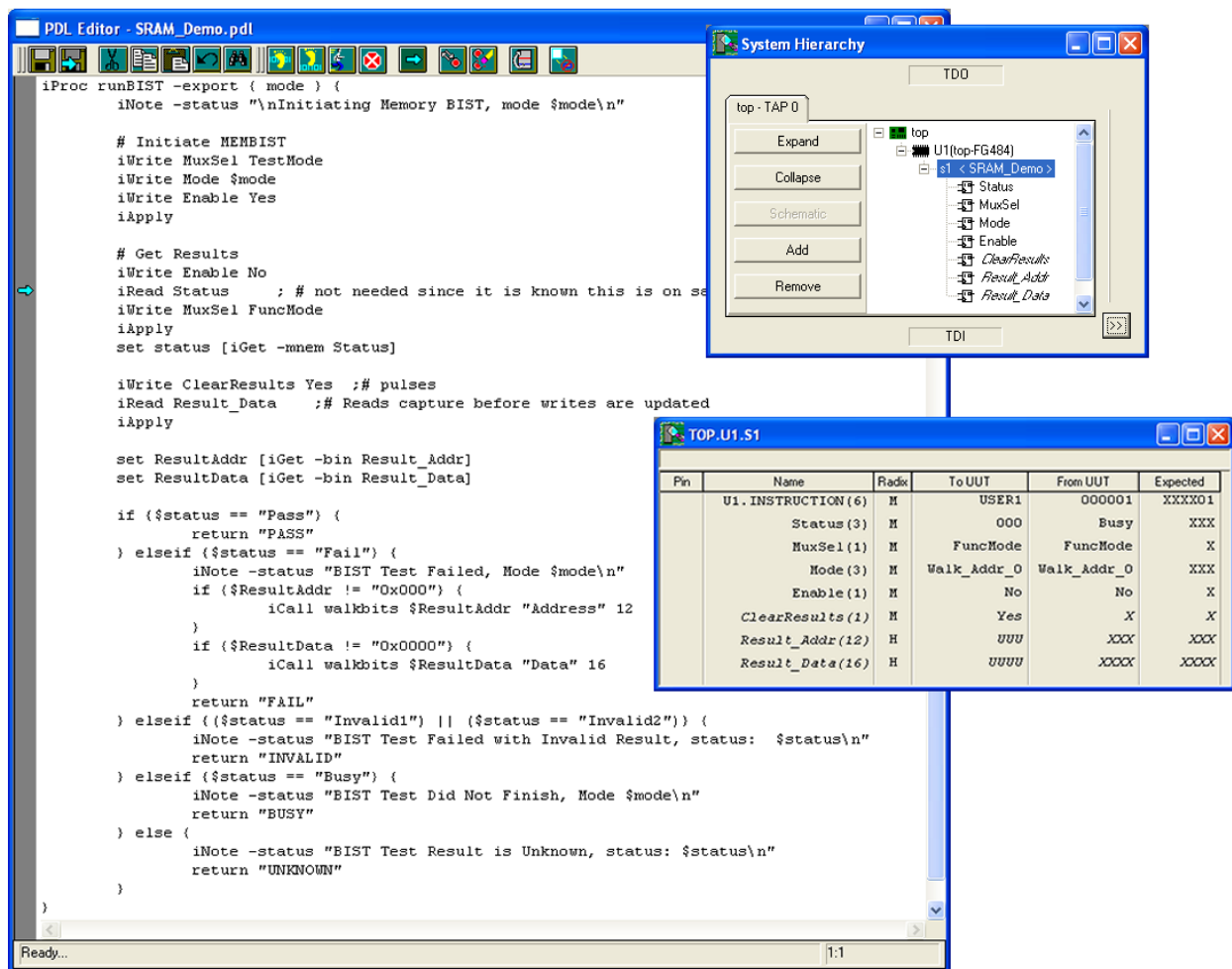
instruments for both ASICs and FPGAs, the TDR interface has to be configurable for both. Note that the **Enable** signal which starts the SRAM BIST must have an update register on it such that it does not toggle during shift operations and it also must reset to the 'disabled' state. In order to optimize the number of scan operations required to communicate to the SRAM BIST, glitch free practices in the design are used. It's possible to write PDL code which uses multiple scans to avoid race conditions but it is better to build wrappers which are glitch free on their own so that interactive GUIs can be used with the instrument. The **MuxSel** signal which switches control from the CPU interface to the 1149.1 interface has an update register and a full TCK cycle delay (as indicated by the D box). The BSDL description for this construct is **DELAYPO** and it is a useful construct when performing multiple operations in a single scan operation while avoiding a race condition. In the diagram, the SRAM BIST mode can be set, the controller enabled and control taken from the CPU all in one scan operation. If the **DELAYPO** construct was not implemented, this is a condition that can be detected by using Questa® simulation.

```
attribute REGISTER_MNEMONICS of SRAM_BIST : package IS
    "ModeVal          (          " &
    "   None          (0b0000), " &
    "   Walk_Addr_0   (0b0001), " &
    "   Walk_Addr_1   (0b0010), " &
    "   Walk_Data_0    (0b0011), " &
    "   Walk_Data_1    (0b0100) " &
    "   ),            " &
    "MuxSelVal        (          " &
    "   TestMode       (0b1),    " &
    "   FuncMode        (0b0)    " &
    "   ),            " &
    "EnableVal        (          " &
    "   Yes            (0b1),    " &
    "   No             (0b0)    " &
    "   ),            " &
    "StatusVal        (          " &
    "   Pass           (0b101),  " &
    "   Fail           (0b011),  " &
    "   Busy           (0bXX0),  " &
    "   Invalid1       (0b001),  " &
    "   Invalid2       (0b111)   " &
    "   )              " ;
attribute REGISTER_FIELDS of SRAM_BIST : package IS
"USER_TDR2[29] ( " &
    "   (ClearResults[1] IS (          28) ResetVal(EnableVal(No)) PULSE1 ), " &
    "   (Result_Addr[12] IS (27 downto 16) NoPO ), " &
    "   (Result_Data[16] IS (15 downto 0) NoPO ) " &
    "   ), " &
"USER_TDR1[8] ( " &
    "   (Status[3]      IS ( 7 downto 5) Captures(StatusVal(-)) NoPO ), " &
    "   (MuxSel[1]       IS (4) ResetVal(MuxSelVal(FuncMode)) Captures(MuxSelVal(-)) DelayPO ), " &
    "   (Mode[3]         IS ( 3 downto 1) ResetVal(ModeVal(None)) Captures(ModeVal(-)) ), " &
    "   (Enable[1]       IS (          0) ResetVal(EnableVal(No)) Captures(EnableVal(-)) ) " &
    "   ) " ;
```

Figure 4. Register definitions for SRAM Test Instrument

The pastel red shaded area in Figure 3 is used to deliver detailed diagnostics about what specifically failed. This section adds 29 bits of additional shift cells which can impact test time. Since it is only necessary to scan this TDR when a failure occurs, the instrument IP is provided with two separate TDRs interfaces. The integrator can access the two TDR segments with different instructions or the integrator can implement a SEGSEL mux inline TDR selector to keep the diagnostic scan chain out of the path.

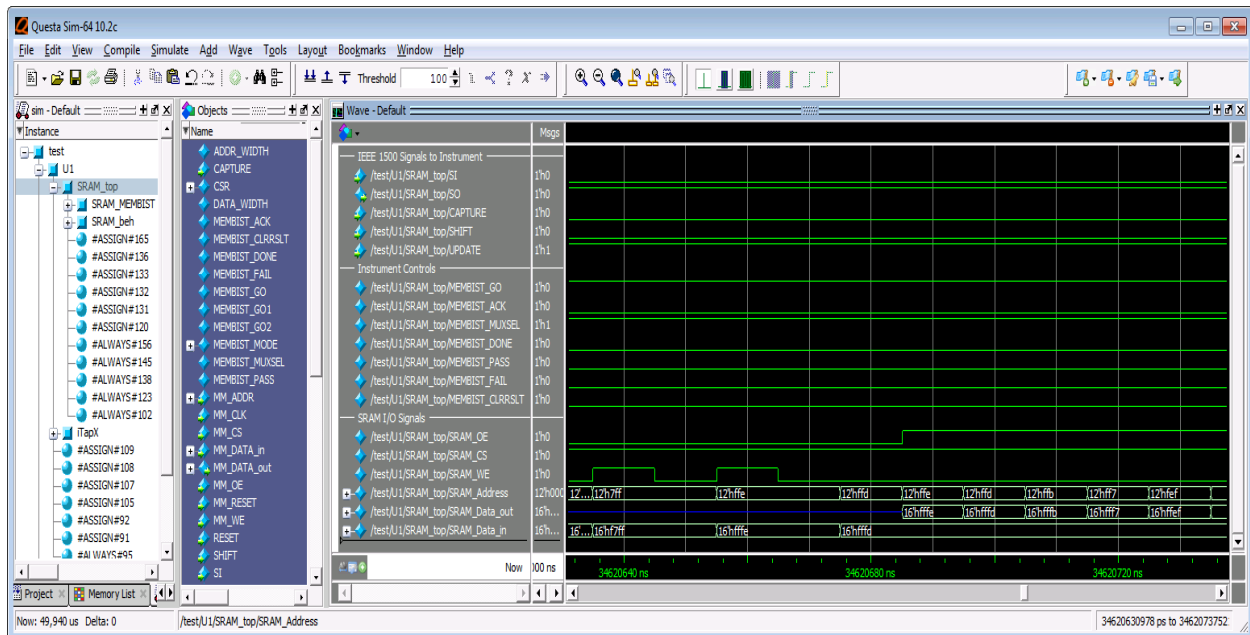
The IEEE 1149.1-2013 standard now includes robust behavioral descriptions of many register cells used in common Design-for-Test practice. Any IEEE 1500 compliant WSP (Wrapper Serial Port) as well as any IEEE 1149.1-2013 power domain segmentation can be described. TDRs are no longer fixed in length and the register descriptions are no longer flat. They have hierarchy and instruments can be defined stand-alone without the need for an IC level BSDL. Figure 4 depicts a code snippet of the BSDL language which describes the register mnemonics and fields of the instrument design in Figure 3.



**Figure 5. Instrument Development Windows**

Figure 5 shows the NEBULA PDL single stepper with hierarchy and register view created automatically from the instrument description and its instantiation as S1 in the design. When PDL routines are executed or single-stepped, each iApply statement causes NEBULA to send scan-in data to the Questa simulator. The response scan-out data from Questa's simulation of the instrument is used to update the internal register representations in the NEBULA software. The NEBULA user can single step the PDL routines and monitor in real-time the TDR bit fields. Early in development of this PDL, Questa® assisted in identifying (See Figure 5) a missing "iRead Result\_Data" command necessary to make sure the Result\_Data and Result\_Address registers are enabled and in the path prior to any iGet command on their contents. The instrument was designed to allow the registers to be on different segments, so the iRead command guarantees that the Result registers were properly scanned prior to the iGet command. A complete source listing of the instrument PDL is available [here](#). (All the files used in this

article, including the Questa® make file are included in the NEBULA download.). The PDL shows the advantage of the instrument provider pre-wrapping their instrument as the MuxSel, Mode and Enable can be set in a single iApply (scan operation) saving test time.



**Figure 6. Questa 1149.1-2013 Instrument Simulation**

Any PDL iProc procedure that needs to be debugged can be done from the NEBULA GUI with Questa® operating on the back end. However, when debugging functional problems of your instrument, the Questa® instrument simulation graphical timing diagram (See

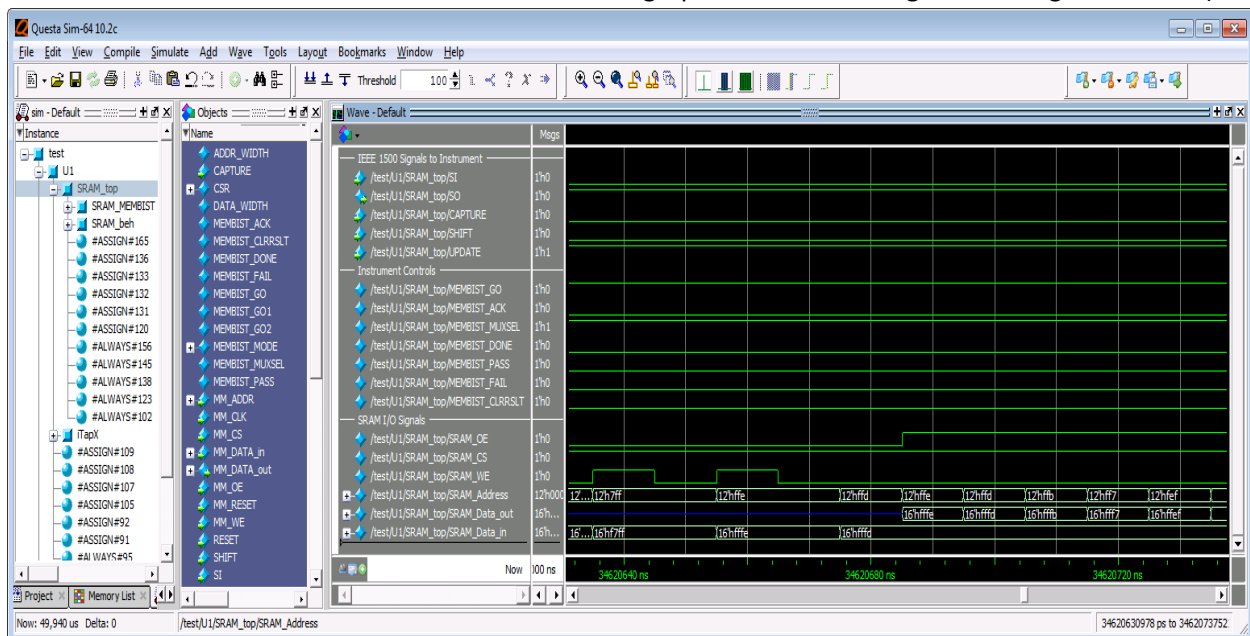


Figure 6) provides needed insight. All instrument internal signals are available for inspection in response to the PDL routines being applied.

A key feature for the 1149.1-2013 PDL developer is the Questa® fault coverage capability. The engineer uses this to validate that the PDL routines are adequately testing the instrument. The coverage report

contains valuable information about unused states or modes as shown in Figure 7. Coverage is improved by adding PDL or removing state machines or logic in the design which may not be necessary.

File: hdl/SRAM_MEMBIST.v				
Enabled Coverage	Active	Hits	Misses	% Covered
-----	-----	-----	-----	-----
Stmts	135	120	15	88.8
Branches	65	56	9	86.1
FEC Condition Terms	0	0	0	100.0
FEC Expression Terms	0	0	0	100.0
FSMs				76.8
States	17	16	1	94.1
Transitions	42	25	17	59.5
Toggle Bins	398	140	258	35.1

**Figure 7. Questa Coverage Report**

## Conclusion

Both Mentor Questa® and Intellitech NEBULA on their own are valuable productivity tools for engineers. Combined they offer a new critical capability that enable pre-silicon validation of silicon instruments for IEEE 1149.1-2013 compliance. Nebula provides the front-end client, processing the instrument package descriptions and PDL operational code. Questa® provides the simulation back end, providing scan responses and code coverage. As with IEEE 1500 wrapped cores, pre-wrapped IEEE 1149.1-2013 instruments offer the best approach to success and low support. Leaving the register creation to the integrator requires the integrator to be aware of race conditions created by the TDR update state and knowledge of how the interface to the instrument works.

A market is already developing with instrument providers creating plug-n-play IEEE 1149.1-2013 pre-validated descriptions and PDL for the ASIC and FPGA market. Up until this time the IP provider has validated using Verilog test benches or loaded designs into FPGAs. With this combined solution instruments can be validated for IEEE 1149.1-2013 compliance much faster and with valuable metrics on code coverage. The best part for the Questa® customer is that this capability can be added without additional software license costs.

## Trademarks

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